

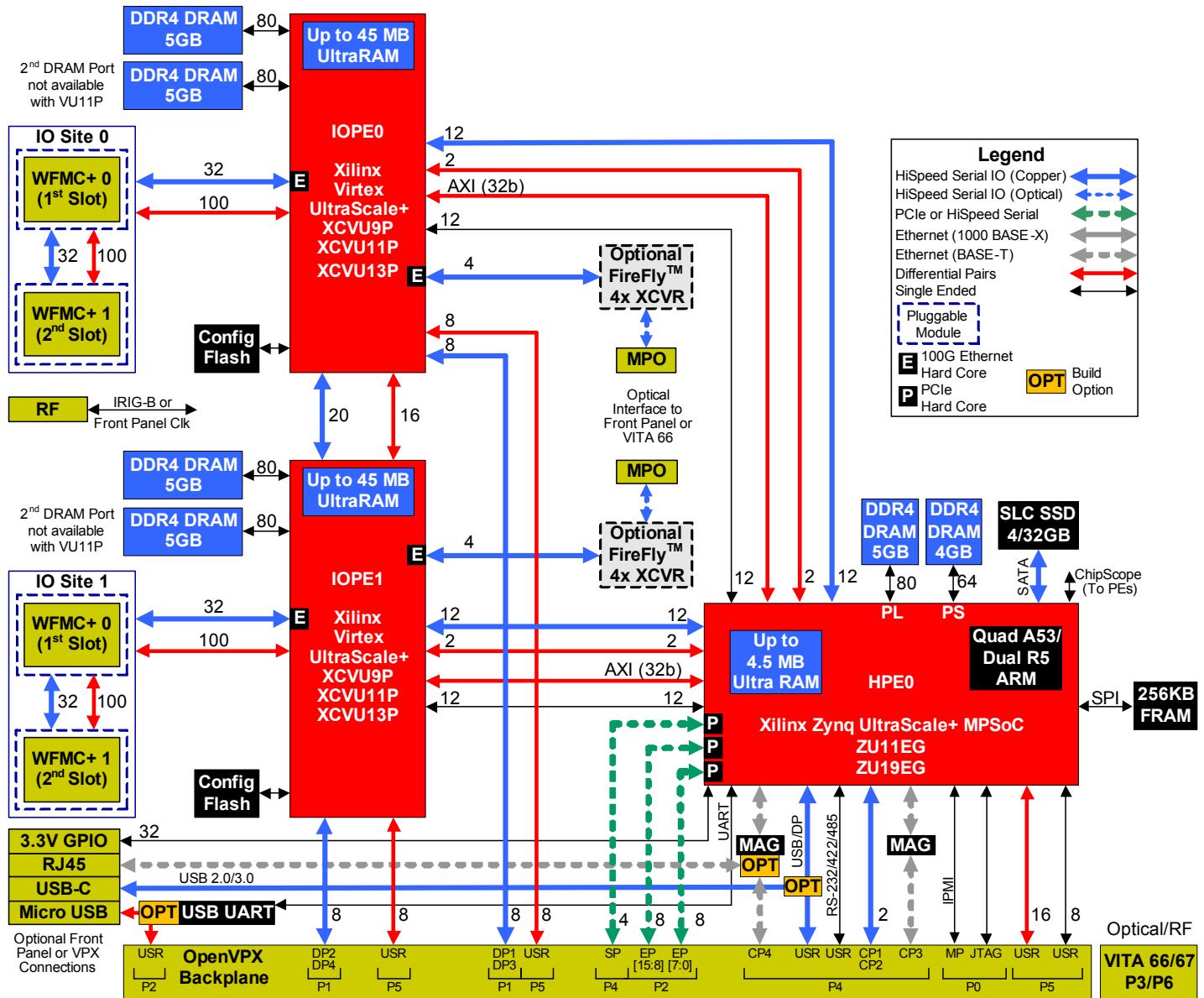
WILDSTAR 6XB2 6U OpenVPX FPGA Processor

The WILDSTAR WB6XB2 6U OpenVPX FPGA Processor combines the processing power of three Xilinx UltraScale+ FPGAs with two configurable high bandwidth WFMIC+ mezzanine sites. This 3rd generation UltraScale+ card was designed from the ground up for extreme environments and builds on Annapolis Micro System's mature 40G EcoSystem to offer 100G capability utilizing 25Gbps+ FPGA transceivers. The on-board 6-core Xilinx MPSoC provides high-performing yet low power self-hosting capability thanks to the power-efficient ARM cores. Add Annapolis' powerful BSP options – which includes free 40GbE IP, support for Xilinx 100GbE hard cores, and both VxWorks 7 and Linux support – and this card is ready for even the most bandwidth intensive applications.



WILD100
EcoSystem

SYSTEM ARCHITECTURE



TWO XILINX® VIRTEX® ULTRASCALE+™ FPGAs

- Supports XCVU9P/XCVU11P/XCVU13P FPGAs
 - Up to 24,576 DSP48E1 Slices and 7,560,000 logic cells
 - Up to 720 Mb of High Bandwidth, Low Latency UltraRAM
 - Gen4 PCIe, 150G Interlaken and 100Gb Ethernet Hard Cores
 - Four 80-bit, 5 GB DDR4 DRAM ports
 - GTH/GTY transceivers operating up to 32.75 Gb/s
 - FPGAs programmable from attached flash, JTAG or Annapolis API
 - 16nm FinFET+ process

ONE XILINX® ZYNQ® ULTRASCALE+™ MPSOC ZU11EG OR ZU19EG MOTHERBOARD CONTROLLER

- Processing Subsystem (PS)
 - Quad-core 64-bit ARM® Cortex-A53
 - Dual-core 32-bit Cortex-R5 real-time processor
 - Mali-400 MP2 graphics processing unit
 - One 64-bit, 4 GB DDR4 memory
 - 4 or 32 GB SLC SATA bulk storage for filesystem
 - 256Kb user SPI FRAM
- Programmable Logic (PL)
 - Up to 2928 DSP slices or 1,143,00 logic cells
 - Up to 36Mb of High Bandwidth, Low Latency UltraRAM
 - Gen4 PCIe, 150G Interlaken and 100Gb Ethernet Hard Cores
 - One 80-bit, 5 GB DDR4 DRAM port
 - GTH/GTY transceivers operating up to 32.75 Gb/s
 - 256Kb user SPI FRAM
- 16nm FinFET+ process
- Provides dedicated AXI bus to IOPE FPGAs for register access
- Board support enabling user customization of ZYNQ+ design
- Multiple levels of hardware and software security

BACKPLANE I/O

- Up to 38 High Speed Serial to VPX Backplane for up to 182 GB/s
- Two 1/10GbE and two 1GbE BASE-T to VPX Control Plane
- 32 LVDS lines to VPX P5, 8 from each IOPE and 16 from HPE
- 8 Single Ended 3.3V I/O to VPX Backplane P5 from HPE
- RS-232, RS-422 or RS-485 interface to ZYNQ HPE
- Backplane Protocol Agnostic connections support 10/40Gb Ethernet, IB capable, AnnapMicro protocol and user designed protocols
- External clock and IRIG-B Support via Backplane
- Radial Backplane Clock Support for OpenVPX backplane signals AUXCLK and REFCLK
 - Allows points-to-point, very high-quality backplane connections to payload cards
 - Allows a system reference clock and trigger from backplane to synchronize and clock compatible ADC/DAC mezzanine cards without front panel connections needed
 - Allows 1000s of analog channels across many backplanes/chassis to be synchronized via backplane



FRONT PANEL I/O

- Two Wild FMC+ (WFMC+) next generation IO sites based on FMC+
 - Accepts standard FMC and FMC+ cards (complies to FMC+ specification)
 - Allows larger form factor Annapolis cards for higher IO density
 - Supports additional LVDS IO for higher density ADC and DAC solutions
 - Supports stacking (2 IO cards per site) when at least one card is WFMC+
 - Up to 32 High Speed Serial and 100 LVDS connections to FPGA
- Simultaneous Optics and ADC/DAC use with two slots (stacked mezzanines)
- One RF (SMA or equivalent) connection capable of input/output
- 2 optional 4x FIREFLY Optical transceivers (optional VITA66)
- USB UART and USB-C with USB 3.0 and DisplayPort. Both can optionally be directed to backplane

APPLICATION DEVELOPMENT BOARD SUPPORT PACKAGE

- Open Project Builder Application Design Suite
 - Full Board Support Package for Fast and Easy Application Development
 - Computational, DSP and Data Flow Control Cores (FFTs, FIR, Math, etc)
 - Develop in GUI environment or create VHDL and use HDL environment
 - Built-in Debugger for Hardware in the loop Debugging
 - Communication Cores Included (10/40Gb Ethernet, AnnapMicro Protocol)
 - VHDL Model includes Source Code for Hardware Interfaces
 - Supports High-Level Synthesis (HLS) Design Flow
- Support for VxWorks 7 or Linux Operating Systems
- VHDL BSP packages including full synthesis and simulation support
- Support for Mathworks HDL Coder™ generated IP
- IOPE JTAG Access through RTM or Ethernet
- Board control and status monitoring can be local (stand-alone), remote (via Ethernet) or hybrid (both local and remote)

MECHANICAL AND ENVIRONMENTAL

- 6U OpenVPX Compliant 1.0" spacing
- Available with +85°C ambient temperature support and -55°C power-on
- Available with -65°C to +105°C storage temperature
- Optional VITA 66/67 support
- Integrated Heat Sink and Board Stiffener
- Available in Industrial Temperature Grades
- Air or Conduction Cooled
- RTM available for additional I/O
- Hot Swappable with air cooled variants
- Only requires +12V and +3.3VAUX from backplane
- Developed in alignment with the SOSA™ Technical Standard
- RT3 backplane connectors for 100G support

STATE-OF-THE-ART PRODUCTION

Our [state of the art production facility](#) is located on site in Annapolis, Maryland, enabling full production of our COTS hardware. Annapolis' manufacturing line is designed to meet customers' needs both large and small, including high mix orders and special manufacturing requirements or timelines. The Annapolis production team enables customers to have long product life-cycle support, and aggressively manages part obsolescence by working closely with customers and continually providing future upgrade paths. Annapolis maintains full part traceability and protects against receipt and use of counterfeit parts.

WILD40/WILD100 EcoSystem

The Wild40/Wild100 EcoSystem for OpenVPX includes [FPGA Boards](#), [WFMC+ Mezzanine Cards](#), [Storage Boards](#), [40GbE/Infiniband Switch Boards](#), [Clock Distribution Cards](#), and [Backplane/Chassis](#). Contact Annapolis Micro Systems for more information or visit our [website](#).

