

Tensilica DNA Processor IP For AI Inference

Industry-leading performance and power efficiency for on-device AI applications

The Cadence® Tensilica® DNA Processors are designed as standalone deep neural network accelerator (DNA) processors to serve demanding and continuously growing artificial intelligence (AI) applications spanning internet of things (IoT), smart home, smartphones, augmented reality (AR) /virtual reality (VR), drones, robotics, surveillance, and automotive – both ADAS and autonomous vehicles (AV).

Overview

On-device AI processing needs span a wide range both in the processing requirements and the types of deep neural networks. There is a need for the processors to be standalone units and scale from low-end IoT applications to high-end automotive applications. The Tensilica DNA processors, including the DNA 100 processor and the Vision C5 DSP, meet these challenges.

Our DNA 100 processor architecture incorporates a hardware engine and a Tensilica DSP. The specialized hardware compute engine inside the DNA 100 processor leverages sparsity for both compute and bandwidth reduction. A single DNA 100 processor can easily scale from 0.5 to 12 effective TMACs, and multiple processors can be stacked to achieve 100s of TMACs for use in the most compute-intensive on-device neural network applications. The Tensilica DSP

will accommodate any new neural network layer that is not currently supported by the hardware engines inside the DNA 100 processor, while also offering the extensibility and programmability of a Tensilica Xtensa® core using Tensilica Instruction Extension (TIE) instructions. The DNA 100 processor can run all neural network layers, including but not limited to convolution, fully connected, LSTM, LRN, and pooling..

DNA 100 Processor Features and Benefits

- Industry-leading performance and power efficiency
 - 2550fps for ResNet50 in a 4K MAC base array configuration
 - Up to 3.4TMACs/W in 16nm
 - Wide and configurable AXI bus width to sustain various ranges of neural network tasks
 - Generic AI processor that runs all neural network layers
 - Integrated DMA
- Architected to serve wide range of compute requirements
 - Single DNA 100 processor scales from 0.5 to 12 effective 8b TMACs
 - Multiple DNA 100 processors can be stacked to achieve 100s of TMACs

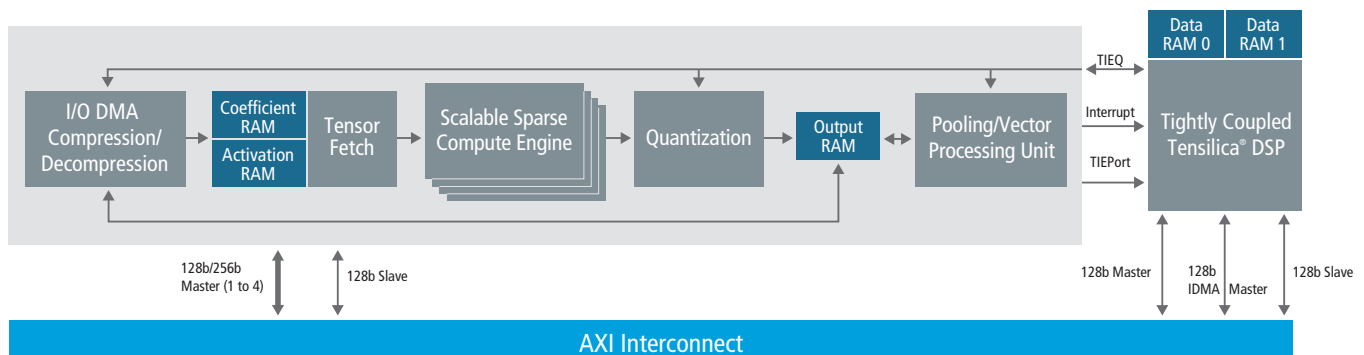


Figure 1: DNA 100 Processor block diagram

- ## Vision C5 DSP Features and Benefits

- ## Toolchain

- A high-performance C/C++ compiler with automatic bundling and vectorization support for the VLIW and SIMD capabilities
- Linker, assembler, debugger, profiler, and graphical visualization tools are included
- A comprehensive instruction set simulator (ISS) allows you to quickly simulate and evaluate performance
- When working with large systems or lengthy test vectors, the fast, functional TurboXim simulator achieves speeds that are 40X to 80X faster than the ISS for efficient software development and functional verification
- Tensilica Xtensa Modeling Protocol (XTMP) for system modeling in C and Xtensa SystemC (XTSC) for system modeling in SystemC® provide for full-chip simulations. The pin-level XTSC model offers co-simulation of the SystemC model at the pin level for fast, cycle-accurate system simulations
- Tensilica Neural Network Compiler maps any neural network trained with a framework such as Caffe, TensorFlow, and TensorFlowLite into executable and highly optimized fixed-point code for target DSPs, leveraging a comprehensive set of hand-optimized neural network library functions
- All major back-end EDA flows are supported

- Cadence Tensilica application engineers can answer your technical questions, and provide technical assistance and custom training.
- Cadence-certified instructors teach a series of courses on Tensilica IP and bring their real-world experience into the classroom.
- Internet Learning Series (iLS) online courses allow you the flexibility of training at your own computer via the Internet.
- The Cadence Tensilica IP support site gives you 24x7 online access to a knowledgebase of the latest solutions, technical documentation, software downloads, and more at ip.cadence.com/support.

