Speedster7t FPGA Datasheet (DS015)

Speedster FPGAs

Achronix®

Data Acceleration

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Chapter - 1: Overview

Introducing the Speedster7t FPGA Family

Achronix's new 7nm Speedster®7t FPGA family is specifically designed to deliver extremely high performance for demanding applications including data-center workloads and networking infrastructure. The processing tasks associated with these high-performance applications, specifically those associated with artificial intelligence and machine learning (AI/ML) and high-speed networking, represent some of the most demanding processing workloads in the data center.

Several performance criteria characterize these data-center and networking workloads:

- The ability to handle high-speed data rates from a host processor's PCIe port and up to 400 Gbps Ethernet ports.
- The ability to store multiple gigabytes of incoming data and to access that data quickly for processing within the FPGA.
- The ability to move massive amounts of data among the FPGA's I/O ports, its internal memory, attached external memory, and its on-chip computing resources.
- The ability to process high computational loads with tera-operations-per-second of performance.

The Speedster7t FPGA family can more than satisfy each of these performance criteria with appropriately scaled and optimized on-chip resources.

Handling High-Speed, Incoming and Outgoing Data

For data-center and networking applications, high-speed data enters an FPGA-based processing node in two fundamental ways: through PCIe connections to a host processor and via high-speed Ethernet connections to other data-center resources. The Speedster7t family is designed to maximize data rates over these connections by implementing a number of PCIe Gen5 interfaces for the host-processor connection(s) and multiple SerDes ports capable of supporting 400 Gbps Ethernet connections. Both of these I/O standards represent the fastest, most recent specifications for inter- and intra-system data communications used in data centers and myriad other FPGA-based applications. The Speedster7t FPGA's multiple, high-speed I/O ports support data rates that data centers expect to see in the near future.

Fast, High-Capacity Memory Storage

Most FPGAs store data that must be accessed quickly in on-chip SRAM. The Speedster7t FPGA family is no exception, incorporating a substantial amount of memory. However, the sheer volume of data that must be handled by many data-center applications almost universally overwhelms any available amount of on-chip SRAM, even when the FPGA in question is fabricated with 7nm FinFET process technology.

Consequently, the Speedster7t is designed with multiple GDDR6 graphics SDRAM ports. In the immediate future, GDDR6 SDRAMs will provide the fastest SDRAM access speeds with the lowest DRAM cost (per stored bit), at power levels equivalent to LPDDR5 SDRAM. Together, these characteristics make GDDR6 SDRAM interfaces the best choice for next-generation system designs. Members of the Speedster7t family support as many as eight independent GDDR6 memory ports.

Massive On-Chip Data Movement

With multiple high-speed PCIe Gen5 and 112 Gbps Ethernet ports combined with GDDR6 SDRAM interfaces, the Speedster7t FPGA family can move a tremendous amount of data directly between these various I/O ports and to the FPGAs' on-chip memory and computational resources. Speedster7t FPGAs employ both the familiar parallel interconnections of earlier FPGA generations and a network on chip (NoC) to facilitate the significantly faster data-transfer rates required by future data centers.

Consider 400 Gbps Ethernet ports, which will become increasingly common in future data centers. An FPGA requires a 724 MHz, 1024-bit internal bus to handle a single, bidirectional 400 Gbps data stream. This wide bus is extremely difficult to route in a conventional FPGA switching fabric based on internal, parallel connections. Now, consider the need to handle multiple 400 Gbps Ethernet ports within a single FPGA — the requirements become even tougher. These are the sorts of data rates that the Speedster7t FPGA's on-chip NoC is designed to handle with ease.

High-Speed, On-Chip Processing Resources

FPGAs excel at processing data at high speeds due to their configurable logic and co-located SRAM resources. The Speedster7t family includes the same processing resources and memories found in previous-generation FPGAs, but adds optimizations and new processing elements to further enhance performance for many applications, including AI/ML applications.

For example, the Speedster7t FPGA incorporates a new resource called machine-learning processor (MLP) blocks, large-scale matrix-vector and matrix-matrix multiplication engines specifically designed to accelerate AI /ML applications. MLP blocks support fixed and floating-point computations, and their resources are fracturable to support the wide range of numerical precision employed by AI/ML applications.

The MLP block architecture has been designed to exploit data-reuse opportunities that are inherent to matrix-vector and matrix-matrix multiplication. This data reuse significantly reduces the amount of data movement among memories, which increases AI/ML algorithm performance while cutting power consumption. In addition, multipliers implemented with the Speedster7t FPGA's lookup tables (LUTs) have been reformulated with the industry's most efficient modified Booth's algorithm, which doubles LUT-based multiplier performance for AI/ML algorithms.

Feature Summary

- MLP blocks with arrays of multipliers, adder trees, accumulators, and support for both fixed and floating point operations
- High-speed SerDes transceivers, supporting 112 Gbps PAM4 and 56 Gbps PAM4/NRZ modulation, as well as lower data rates
- Hard Ethernet MACs that support up to 400G
- Multiple PCIe Gen5 ports
- Network-on-Chip (NoC) enabling high-bandwidth data flow throughout and between the FPGA fabric and hard I/O and memory controllers and interfaces
- GDDR6 and DDR5 SDRAM controllers and interfaces (AC7t1500 supports DDR4 rather than DDR5)
- New logic architecture with 6-input LUTs (6LUT), 8-bit ALUs, flip-flops, and a reformulated multiplier LUT (MLUT) mode based on a modified Booth algorithm, which doubles the performance of LUT-based multiplication
- Fabric routing enhanced with dedicated bus routing and active bus muxing
- 72 kb BRAM and 2 kb LRAM Memory blocks

- GPIO supporting multiple I/O standards
- PLLs and DLLs to support multiple, on-chip clock trees
- Support for multiple types of programming interfaces
- Partial reconfiguration of the FPGA fabric
- Remote update of the FPGA fabric
- Security features for encrypting and authenticating bitstreams
- Debug support through Achronix's Snapshot

Family Features

Table 1: ***Speedster7t Family Overview***

Features	AC7t750	AC7t1500	AC7t3000	AC7t6000
6-input LUTs	363K	692K	1.3M	2.6M
Embedded memory	100 Mb	190 Mbit	192 Mbit	385 Mbit
MLP blocks	336	2,560	880	1,760
SerDes 112Gbps (LR + XSR)	24 + 16	32 + 0	40 + 32	72 + 0
Dedicated GPIO	32	64	50	100
Additional GPIO	150	150	300	600
DDR5 channels	1	1†	2	4
GDDR6	8 channels	16 channels ‡	16 channels	16 channels
PCIe Gen5	One ×16	One ×16 and one ×8	One ×16 and one ×8	Two ×16
Ethernet	8 lanes, 2×400G or 8×100G	16 lanes, 4×400G or 16×100G	16 lanes, 4×400G or 16×100G	32 lanes, 8×400G or 32×100G

Note

† AC7t1500 supports DDR4.

‡ This option varies by package size, see the table **Speedster7t Package and I/O Combinations** for more details.

Table 2: ***Speedster7t Package and I/O Combinations***

Package Dimensions (mm)	AC7t750	AC7t1500	AC7t3000	AC7t6000
	GDDR6, SerDes, GPIO	GDDR6, SerDes, GPIO	HBM2, SerDes, GPIO	HBM2, SerDes, GPIO
45×45	8 channels, 32, 32	8 channels, 32, 64		
52.5×52.5		16 channels, 32, 64	16 channels, 72, 50	16 channels, 72, 100

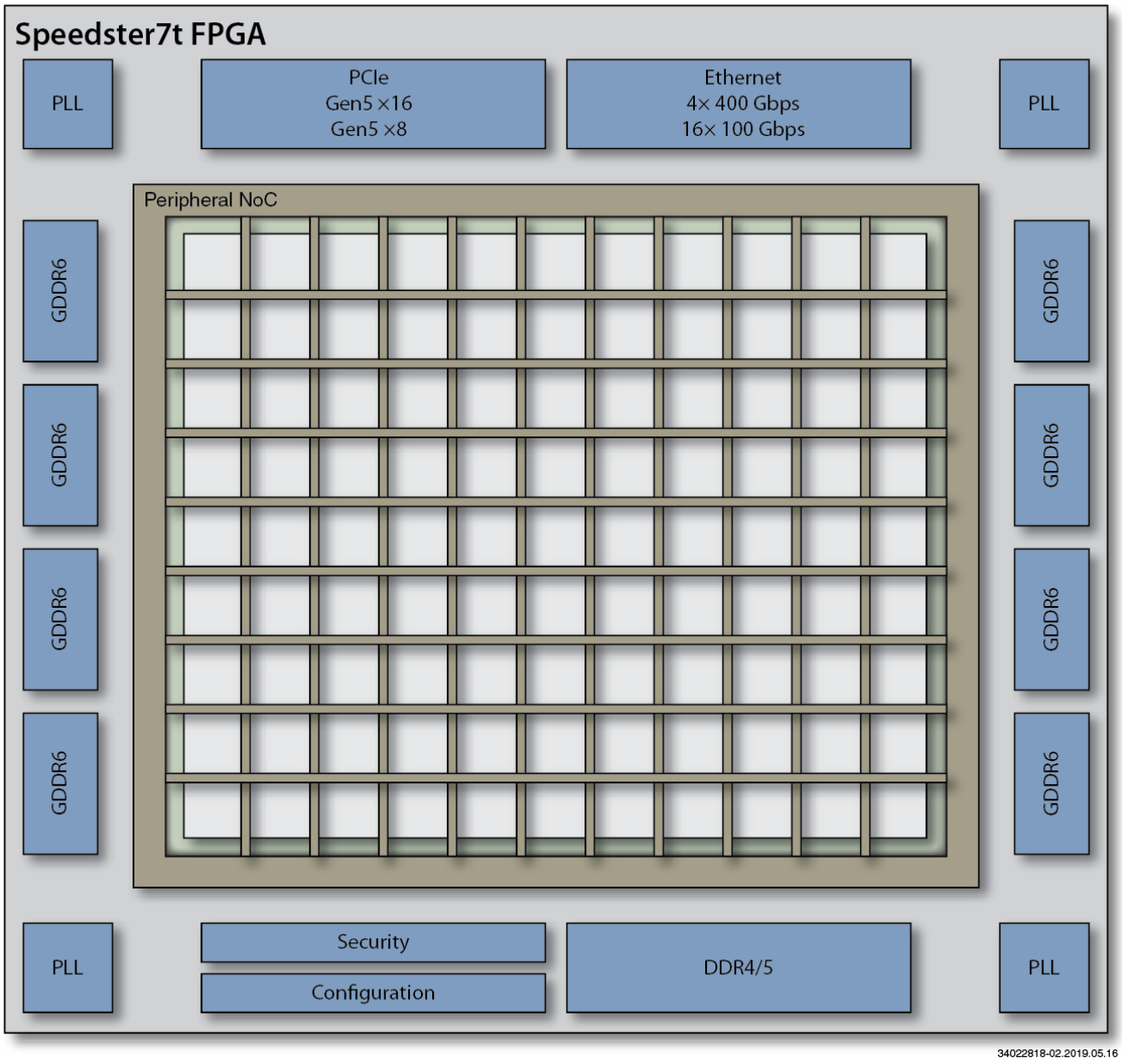

Figure 1: ***Speedster7t1500 Top-Level Block Diagram***

Chapter - 2: Speedster7t Fabric Architecture

The Speedster7t FPGA fabric is optimized for artificial intelligence and machine learning applications as well as hardware acceleration. The fabric is comprised of two main tile types: reconfigurable logic blocks (RLBs) that contain look-up tables, flip-flops, and ALUs, and machine learning processing (MLP) blocks that contain multipliers, adders, accumulators, and memory. The tiles are distributed as columns in the Speedster7t FPGA, and each tile consists of a routing switch box plus a logic block.

Fabric Clock Network

Speedster7t FPGAs have two types of clock networks targeted to provide both the low-skew, balanced architecture as well as addressing the source-synchronous nature of data transfers with external interfaces.

The global clock network is the hierarchical network that feeds resources in the FPGA fabric. The global clock trunk runs vertically up and down the center of the core, sourced by global clock muxes at the top and bottom of the global trunk. The global clock network uses low-latency and low-skew distribution techniques to reach all possible endpoints in the FPGA fabric.

The second clock network, available at the periphery of fabric, is the interface clock network. As the name implies, the intent of these clocks is to facilitate the construction of interface logic within the FPGA fabric operating on the same clock domain as external logic. Specifically, interface clocks drive the logic that communicates with the hard IP interfaces on a Speedster7t device. Interface clocks are optimized for low latency and drive logic within a specific area in the FPGA fabric.

Achronix provides dedicated clock dividers, glitch-less clock switches, and clock gates for ease of use in a customer's design. Additionally, ACE automatically provides support for inserting programmable delays at various points on a clock path to increase performance and easily facilitate timing closure.

Fabric Routing

Global Interconnect

All the tiles in the fabric are connected through the global interconnect, allowing for routing between elements. The switchboxes in each tile are the connection points between vertical and horizontal routing tracks. In addition to the traditional per-signal routing, the Speedster7t FPGA family introduces bus routing for high-performance data paths.

Bus Routing

The Speedster7t FPGA includes both traditional per-bit routing, as well as dedicated bus routing. The Speedster7t FPGA architecture includes separate dedicated bus-based routing for high-performance datapaths. These buses are placed into groups of up to 8 bits wide and are routed independently from standard routing in order to significantly reduce congestion.

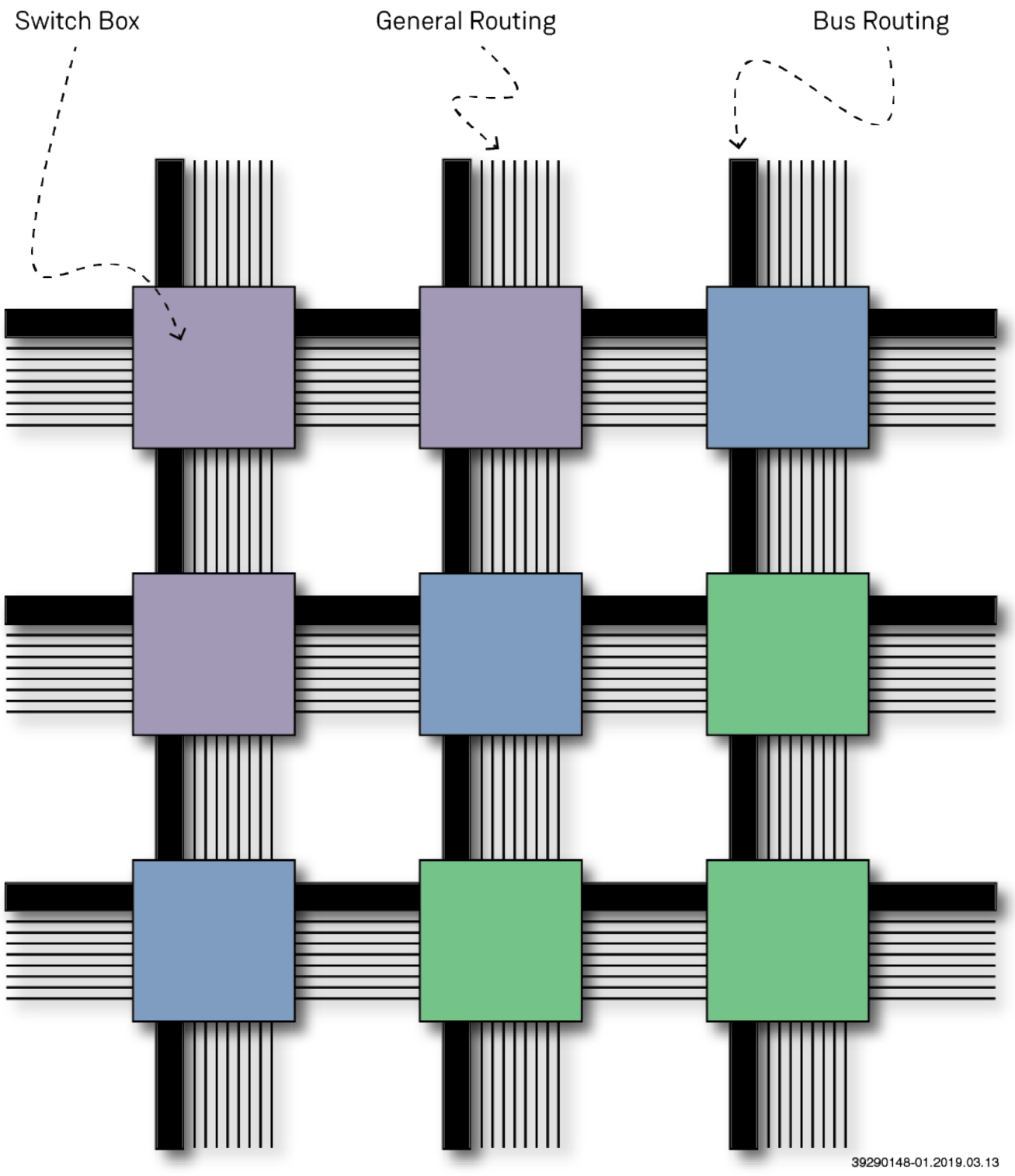

Figure 2: ***Speedster7t Bus Routing***

Additionally, the Speedster7t FPGA architecture introduces a programmable switch network for bus routing. There is a 4 × 1 bus MUX for each of the 8-bit buses inside each Speedster7t switchbox. These bus MUXes are cascadable for wider MUX requirements. This added MUXing reduces overall logic and routing resources for a design, leading to improved performance and smaller area.

Reconfigurable Logic Block (RLB)

An RLB contains 6-input look-up-tables (LUT-6), each with two optional registers and an 8-bit fast arithmetic logic unit (ALU). The table below provides information on the resource counts inside an RLB in the Speedster7t FPGA.

Table 3: *RLB Resource Counts*

Resource	Count
6-LUTs	12
Registers	24
8-bit ALU	3

The following features are available using the resources in the RLB:

- Support for LUT chaining within the same RLB and between RLBs
- 8-bit ALU for adders, counters, and comparators
- MAX function that efficiently compares two 8-bit numbers and chooses the maximum or minimum result
- Dedicated connections for high-efficiency shift registers
- Multiplier LUT (MLUT) mode for efficient multipliers
- Ability to fan-out a clock enable or reset signal to multiple tiles without using general routing resources

MLUT Mode

The RLB includes an MLUT mode for an efficient LUT-based multiplication. MLUT mode results in 2 × 4 multiplier building blocks being configured that can be stacked horizontally and vertically to generate any size signed multiplier. For example, a 2 × 8 multiplier building block can be generated with two 6-LUTs; one RLB6 can perform a 6 × 6 multiply.

Note

MLUT mode is supported by the MLUT generator within ACE to help customers build the multiplier desired.

Machine Learning Processing (MLP) Block

The machine learning processing block (MLP) is an array of up to 32 multipliers, followed by an adder tree, an accumulator, and a rounding/saturation/normalize block.The MLP also includes two memory blocks, a BRAM72k and LRAM2k, that can be used individually or in conjunction with the array of multipliers. The number of multipliers available varies with the bit width of each operand and the total width of input data. When the MLP is used in conjunction with a BRAM72k, the amount of data inputs to the MLP block increases along with the number of multipliers available.

The MLP offers a range of features including integer multiply with optional accumulate, bfloat16 operations, floating point 16, block floating point, and floating point 24. Below is a list of features available with the MLP block:

- Configurable multiply precision and multiplier count
  - Up to 32 multiplies for 4-bit integers or Block float 12 in a single MLP
  - Up to 16 multiplies for 8-bit integers or Block float 16 in a single MLP
  - Support for 16-bit integer, Bfloat16, Floating point 16, and Floating point 24 in a single MLP
- Multiple number formats (fixed and floating point)
- Deep adder tree and accumulator block
- Multiple rounding and saturation features
- Tightly coupled circular register file (LRAM) for easily caching and feeding back results
- Tightly coupled BRAM for reusable input data such as kernels or weights
- Cascade paths up a column of MLPs
  - Allows for broadcast of operands up a column of MLPs without using up critical routing resources
  - Allows for adder trees to extend across multiple MLPs
  - Broadcast read/write to tightly coupled BRAMs up a column of MLPs to efficiently create large memories

Along with the numerous multiply configurations, the MLP block includes optional input and pipelining registers at various locations to support high-frequency designs. There is a deep adder tree after the multipliers, with the option to bypass the adders and output the multiplier products directly. There is a normalization block for floating-point and block-floating-point operations. In addition, a feedback path allows for accumulation within the MLP block.

Below are block diagrams showing the MLP using the fixed or floating-point formats.

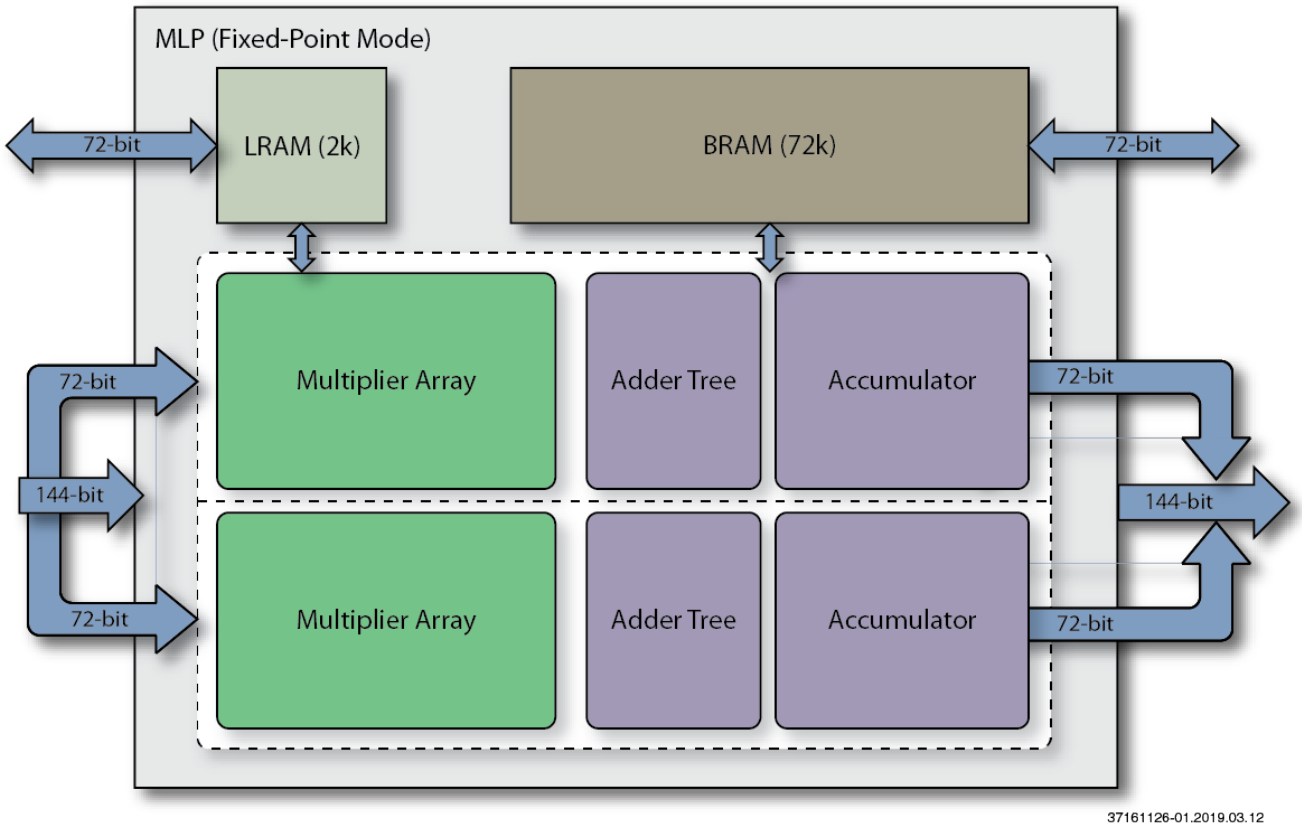

Figure 3: ***MLP Using Fixed-Point Mode***

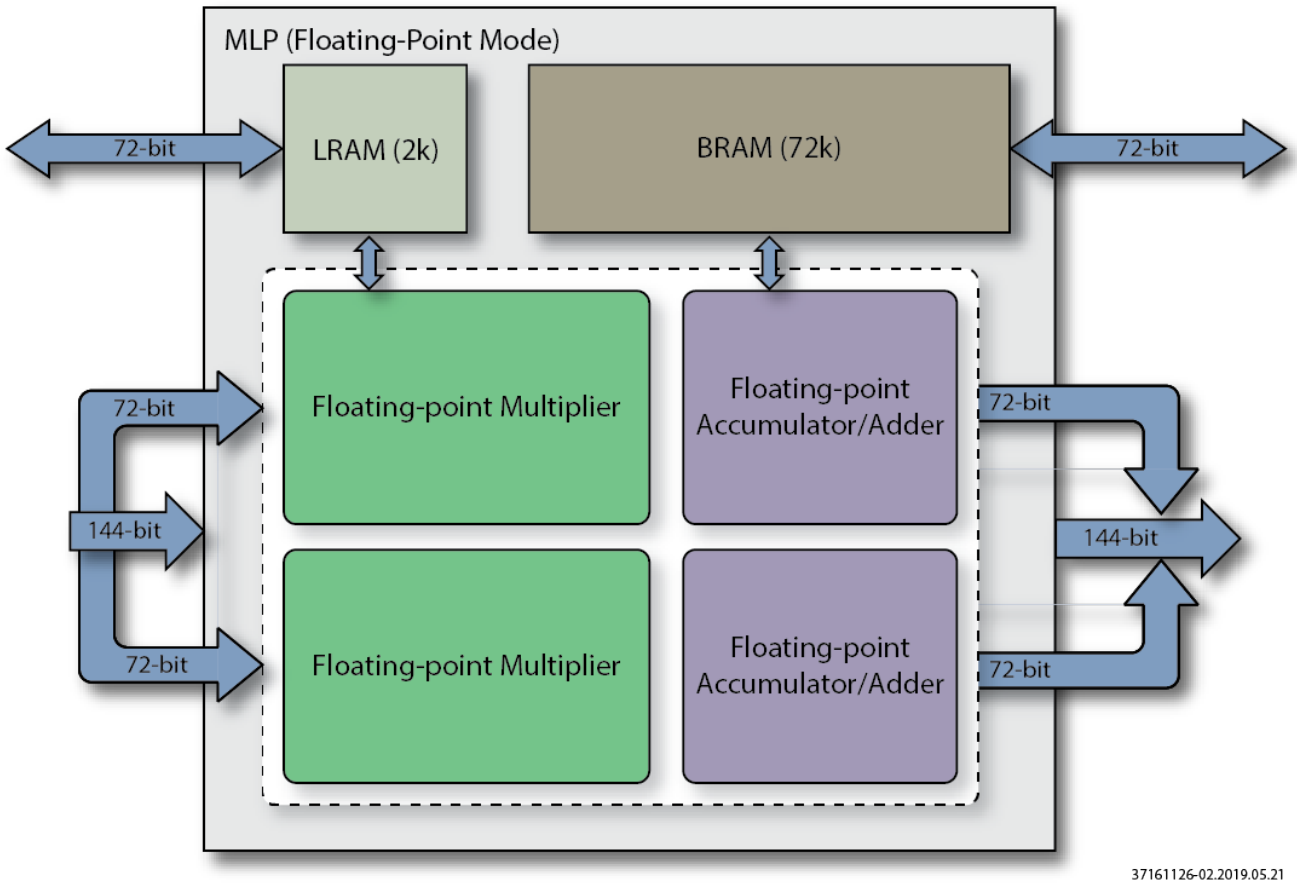

Figure 4: ***MLP Using Floating-Point Mode***

A cascade path allows for the adder tree to extend across multiple MLP blocks in a column without using extra fabric resources, and a data cascade/broadcast path is available to send operands across multiple MLP blocks. Below is a diagram showing the cascade paths across MLPs.

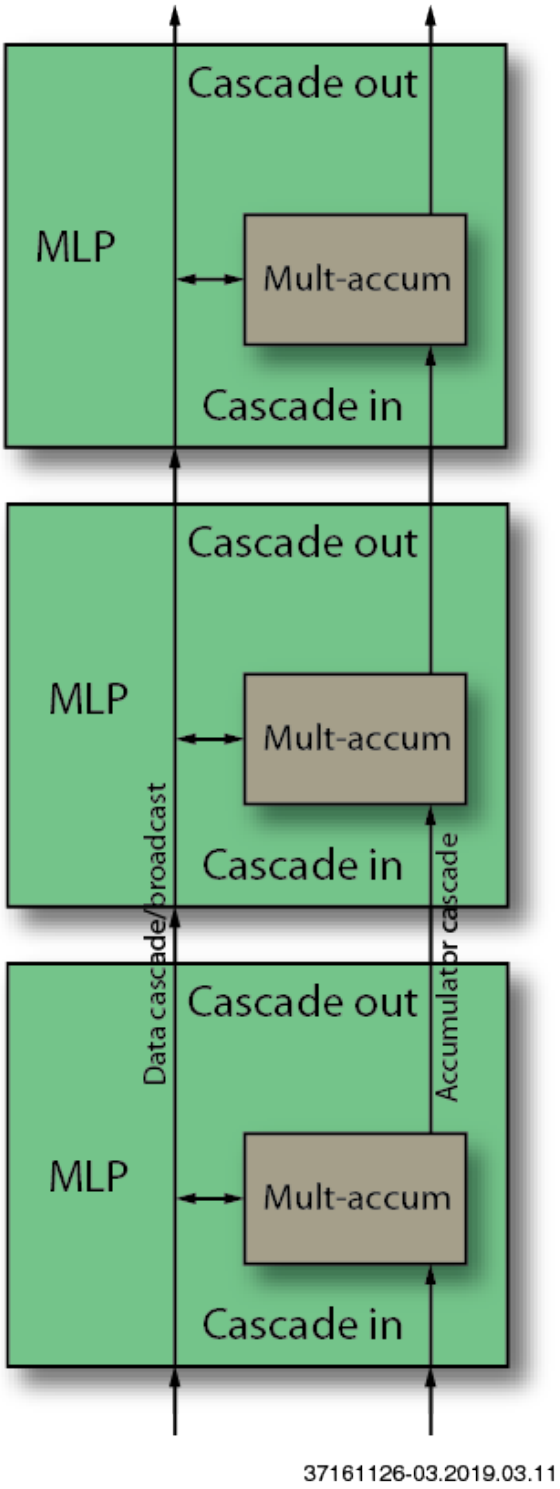

Figure 5: ***MLP Cascade Path***

Block RAM 72k (BRAM72k)

The BRAM72k primitive implements a 72-kb simple-dual-port (SDP) memory block with one write port and one read port. Each port can be independently configured with respect to size and function, and can use independent read and write clocks. The BRAM72k can be configured as a simple dual port or ROM memory. The key features (per block RAM) are summarized in the table below.

Table 4: *BRAM72k Key Features*

Feature	Value
Block RAM size	72 kb
Organization	1024 × 72, 2048 × 36, 4096 × 18, 8192 × 9, 16384 × 4
Physical Implementation	Columns throughout device
Number of Ports	Simple Dual Port (independent read and write)
Port Access	Synchronous writes, synchronous reads, write and read clock can be asynchronous to each other
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

The BRAM72k ports are Illustrated in the following figure:

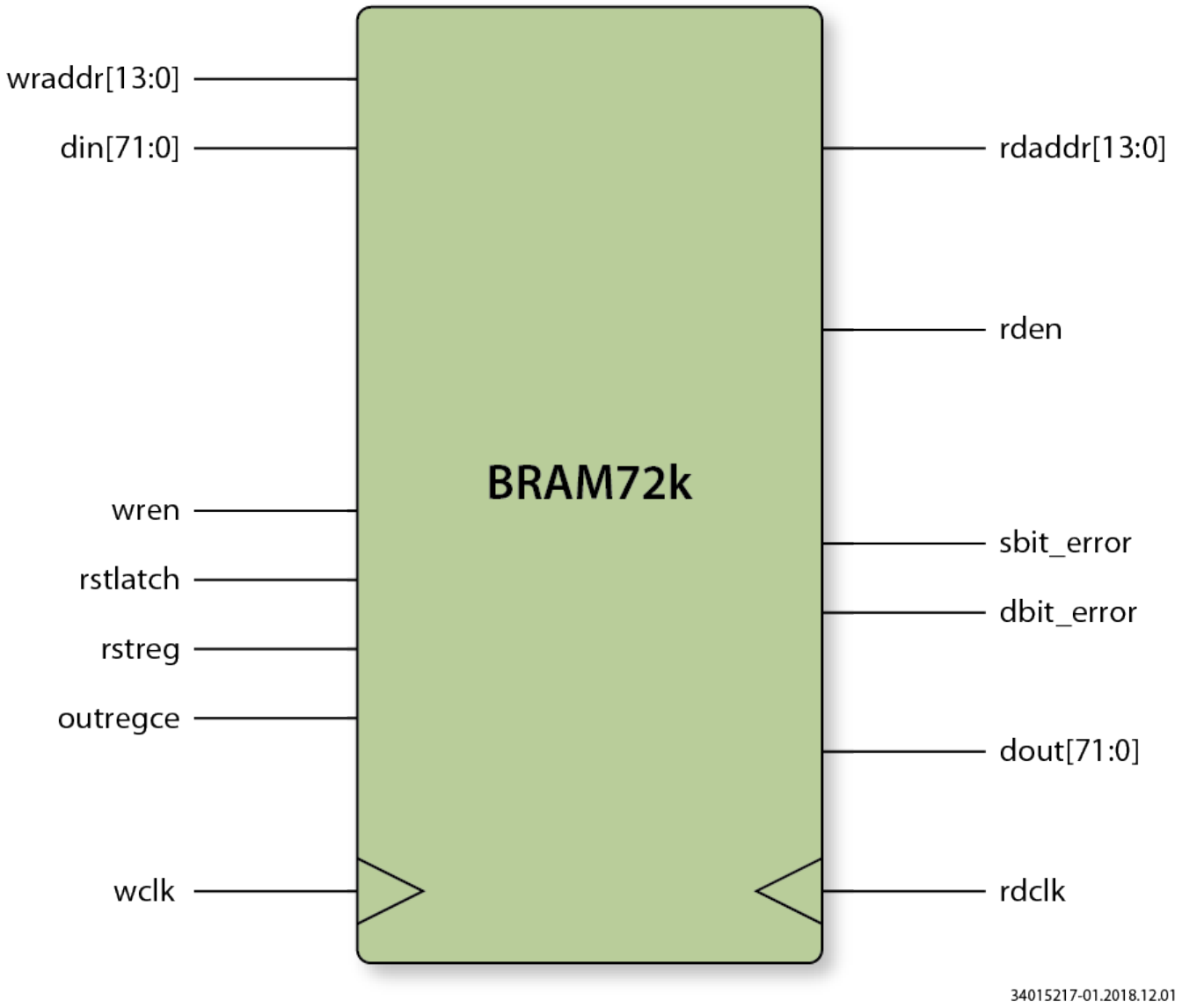

Figure 6: ***BRAM72k Block Diagram***

Logic RAM 2k (LRAM2k)

The LRAM2k implements a 2,304-bit memory block configured as a 32 × 72 simple dual-port (one write port, one read port) RAM. The LRAM2k has a synchronous write port. The read port is configured for asynchronous read operations with an optional output register. This memory block is distributed in the eFPGA fabric. A summary of LRAM2k features is shown in the table below.

Table 5: *LRAM2k Key Features*

Feature	Value
Logic RAM size	2,304 bits
Organization	32 × 72, 64 × 36, 16 × 144(†) (depth × width)
Physical Implementation	Columns throughout device
Number of Ports	Simple dual port (one read, one write)
Port access	Synchronous writes, combinatorial reads
FIFO	Built-in FIFO controller with dedicated pointer and flag circuitry

Note

† 16 × 144 only available as internal path when tightly coupled with MLP.

The LRAM2k ports are shown in the following figure:

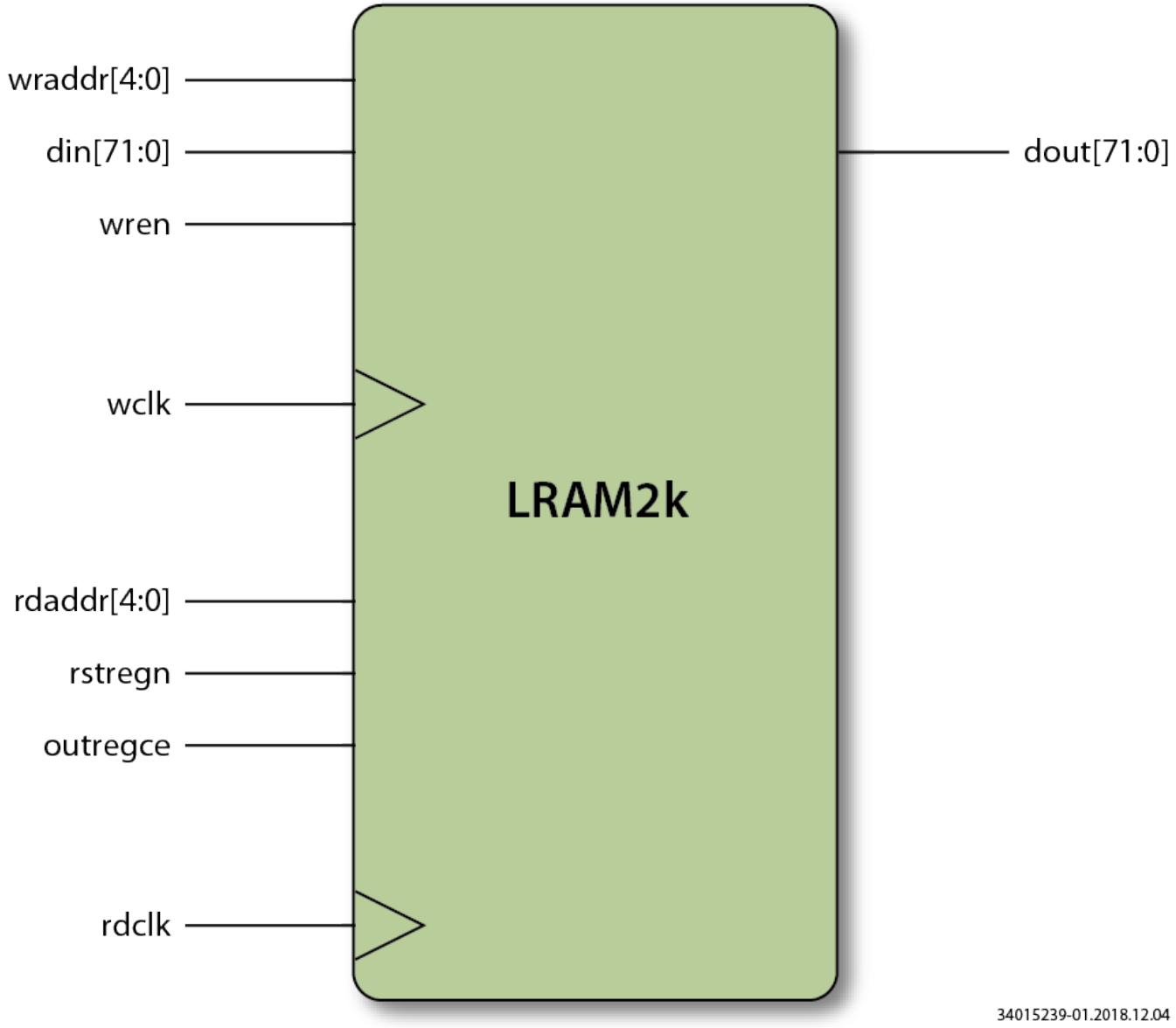

Figure 7: ***LRAM2k Block Diagram***

Chapter - 3: Speedster7t FPGA I/O and PHY

Speedster7t FPGAs have a variety of I/O and PHY to communicate with external components.

112 Gbps SerDes

Speedster7t FPGAs provide high-speed serial transceivers which can be used for interface protocols running from 1 Gbps up to 112 Gbps. They are designed to support NRZ and PAM data-center standards. The Speedster7t FPGA provides a PCS and PMA to support the needs of many common high-speed serial protocols.

PMA Features

- Data rates from 1 Gbps to 112 Gbps
- DC coupling or external AC coupling
- Lock to reference clock or data
- Support for oversampling
- BIST with near/far-end loopback and PRBS 7, 13, 15, 23, 31 generator/checker
- Eye monitor

PCS Features

- Data rates from 1 Gbps to 112 Gbps
- Supports data path widths of 16, 20, 32, 40, 64, and 128 bits
- 8b/10b encoding/decoding support for PCIe 16, 20, and 32-bit internal data paths
- Comma detection and byte/word alignment for PCIe 8b/10b
- 128b/130b encoding/decoding support for PCIe Gen3/Gen4/Gen5 32 and 64-bit internal data path
- Elastic receive buffer for clock compensation and channel bonding
- Support for 66b/64b CAUI gearbox in both synchronous and asynchronous mode
- Support for 67b/64b gearbox in synchronous mode
- Native support for Ethernet 1G/10G/25G/50G/100G, XAUI, CPRI, Jesd4C, SyncE, and Interlaken
- Bypass mode for PCS (bypasses the PCS)

GPIO

Speedster7t FPGAs provide two types of general-purpose I/O (GPIO) pins to enable communication with external components:

- MSIO – Single-ended GPIO that support multiple I/O standards at multiple voltages.
- DIFF-IO – Differential GPIO that support LVDS and LVPECL standards. These are appropriate for connecting high-quality clock inputs.

Below is a table listing the supported I/O standards for each GPIO type.

Table 6: *Supported I/O Standards*

I/O Type	I/O Standard Supported
MSIO	1.8V LVCMOS
	1.5V LVCMOS
	1.2V LVCMOS
	1.1V LVCOMS
	SSTL-18 Class I & 2
	SSTL-15 Class I & II
	SSTL-15
	SSTL-135
	SSTL-12 Class I
	1.8V HSTL Class I & II
	HSUL-12
	Differential SSTL-18 Class I & II
	Differential SSTL-15
	Differential SSTL-135
MSIO	Differential SSTL-12
	Differential HSUL 12
DIFF-IO	1.8V LVCMOS
	1.5V LVCMOS
	LVDS
	LVPECL

DLL

The programmable DLLs provide precise phase alignment between output clocks, deskew signals relative to a clock, and includes features such as spread-spectrum support. Below is a list of features supported in the programmable DLLs.

- Supports 300-1333 MHz
- 256 taps
- Full UI range
- Supports dynamic reconfiguration, making it possible to change taps at runtime
- Supports duty-cycle distortion (DCD) ±2% of reference clock period
- Supports power-down mode when not used in the design
- Lock detection
- Supports holding DLL in reset
- At-speed scan testing
- Available output test clock
- Control and status register read back

PLLs

There are sixteen general purpose PLLs, four in each corner of the Speedster7t FPGA. They are fractional-N divide and spread-spectrum PLLs, supporting a wide range of frequencies with excellent jitter performance. The general-purpose PLLs can be used to drive low-skew, high-speed clocks to nearby I/O, the global clock network, and interface clocks in the FPGA fabric.

Below is a list of features available in the PLLs:

- Programmable PLL with fractional-N divide and spread-spectrum clock generation
- Wide range of output frequencies supported: 100 MHz to 4 GHz
- Up to four input reference clocks from dedicated clock I/O, adjacent PLLs (for cascading PLLs), as well as clock pins and PLLs from other device corners
- Reference clock and output clock dividers range from 1-128
- Low jitter
- Low power

Table 7: *Details of PLL*

Parameter	Min	Max	Units
Reference frequency	10	600	MHz
Output frequency	100	4000	MHz
Output duty cycle	48	52	%

Parameter	Min	Max	Units
Maximum long-term jitter	±2% divided reference clock		

Chapter - 4: Speedster7t FPGA Network On Chip

The Speedster7t FPGA family of devices have a network hierarchy that enables extremely high-speed dataflow between the FPGA core and the interfaces around the periphery, as well as between logic within the FPGA itself. This on-chip network hierarchy supports a cross-sectional bidirectional bandwidth of 20 Tbps. It supports a multitude of interface protocols including GDDR6, DDR4, 400G Ethernet, and PCI Express Gen 5 data streams, while greatly simplifying access to memory and high-speed protocols. Achronix's network on chip (NoC) provides for read/write transactions throughout the device, as well as specialized support for 400G Ethernet streams in selected columns.

Master Endpoints

- 80 network access point (NAP) masters distributed throughout the FPGA core for user-implemented masters
- 2x PCI Express Interfaces
- Fabric configuration unit (FCU)

Slave Endpoints

- 80 NAP slaves distributed throughout the FPGA core for user-implemented slaves
- 16x GDDR6 slave interfaces
- DDR4 controller
- 2x PCI Express Interfaces
- All control and status register (CSR) interfaces of all IP cores
- FCU (to enable configuring of FPGA and interface IP subsystems)

Packet Endpoints

- 2x Ethernet subsystems, supporting a mix of up to 4x 400Gbps Ethernet or 16x 100Gbps Ethernet
- 80 NAP packet interfaces distributed throughout the FPGA core, 32 of which can send and receive data to /from the Ethernet subsystems

NoC Features

The NoC provides a method to easily connect high-bandwidth interfaces to the FPGA fabric, as well as enabling communication between memory and high-speed protocols. To make these high-bandwidth connections both flexible and easy to use, the NoC provides the following features.

Table 8: *Network on Chip (NoC) Features*

Feature Summary	Feature Description
NoC-FPGA Interface Modes	The NoC-to-FPGA access point (NAP) supports the following modes: • AXI 256b slave mode • AXI 256b master mode • Ethernet packet mode • NAP-to-NAP transfer mode
NoC Memory Address translation and firewall	The NoC implements an address translation table for each NAP. This allows the FPGA design to control how the global memory space is arranged for each NAP, and allows access to specific memory regions to be blocked for security, also on a per-NAP basis.
NoC forwarding Latency	1ns to 1.5ns of latency per hop.
NoC Flow Control	The NoC manages flow control internally, such that data is never dropped. Users have the option to implement their own flow control mechanism to control congestion and latency.
NoC Security	The NoC implements address translation tables to support security.

The NoC extends both vertically and horizontally until reaching the edge of the device. The diagram below shows the connections between the peripheral portion of the NoC, the high-bandwidth interfaces, and the columns and rows of the NoC. As shown, the Ethernet has dedicated connections of up to 400G to specific columns of the NoC. The PCIe ×16 and ×8 connect to the periphery of the NoC at 512 Gbps and 256 Gbps respectively. For GDDR6, the NoC can achieve bandwidth of up to 2 Tbps over the full group of GDDR6 interfaces on each side of the device. The columns and rows of the NoC can move traffic to/from the user logic in the fabric at up to 512 Gbps in each direction.

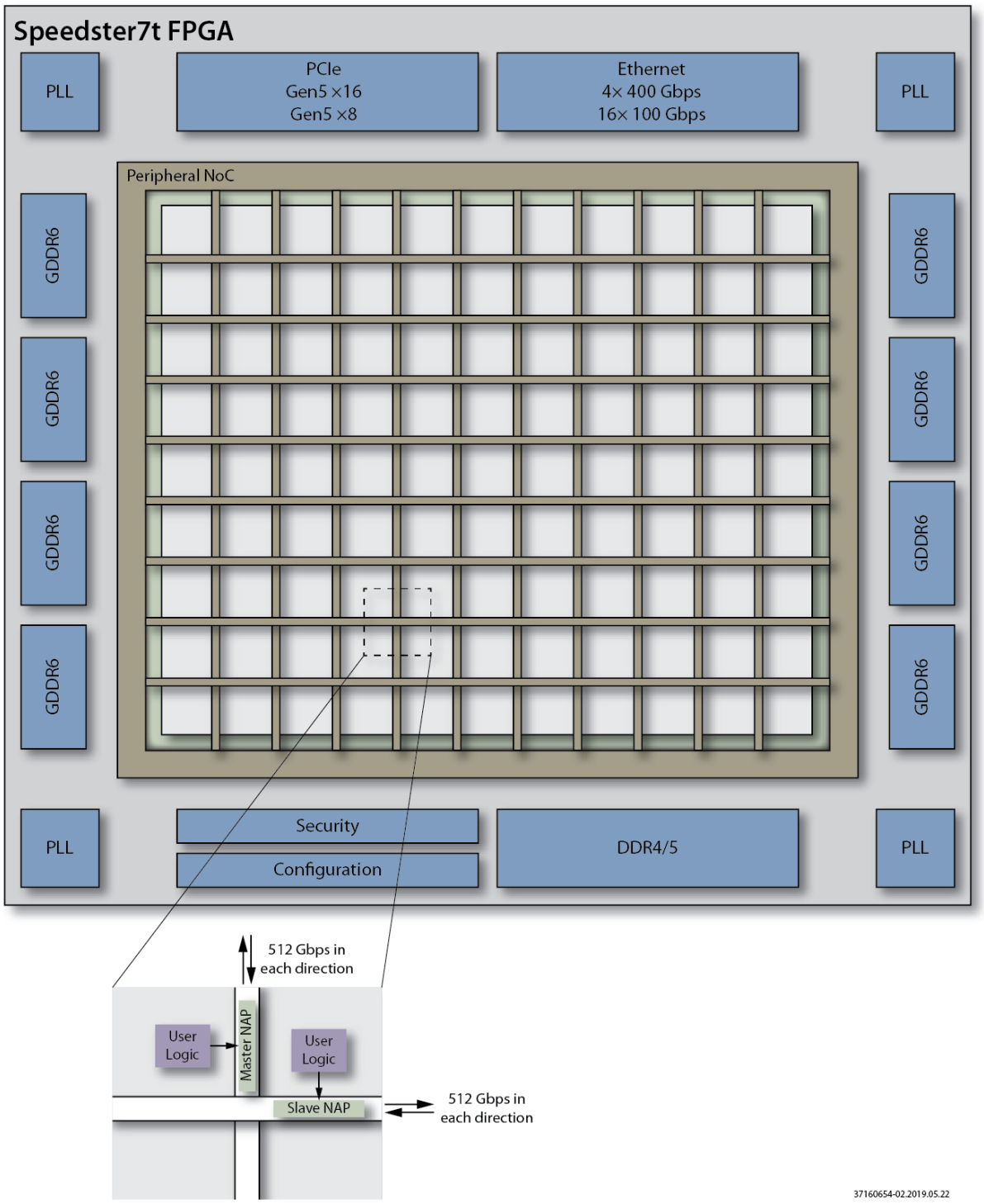

Figure 8: ***Speedcore7t NoC Showing Master and Slave Endpoints***

Columns and Rows of the NoC

The NoC is composed of regularly spaced node elements at the center of each cluster throughout the core fabric of the FPGA. The NoC nodes provide connectivity to adjacent nodes in both the horizontal and vertical directions. Each horizontal and vertical link within the NoC supports 512 Gbps throughput in both directions.

The NoC transaction mapping logic is optimized for AXI read and write transactions. User master logic implemented in the FPGA core can issue AXI read or write transactions to the NAP's AXI slave, and the NoC row carries the transaction to the east or west boundary of the FPGA core to be issued to the deep DDR4/5 memory interface or one of the high-speed GDDR6 memory interfaces. PCIe transactions arriving from the north side of the device are issued to the NoC columns, which transport the transaction requests down the columns to user slave logic in the FPGA.

Each row and column is able to support a full 512 Gbps of traffic.

The rows and columns of the NoC support both transactional and non-transactional data transfers such as streams of packet data.

- **Transactional data transfer** – This type of transfer includes read and write commands, data, and responses. The command transfers are typically a single cycle, and data transfers are typically short, with 4-cycle transactions being very common.

- **Non-transactional data transfer** – There are two kinds of non-transactional type data transfer
    - Packet – This transfer allows data to be bundled as longer streams of data. The NoC imposes no upper limit on packet sizes.
    - NAP-to-NAP – The NoC allows the user to send data between NAPs within the same column or the same row. In this mode, flow control units (flits) are transferred from endpoint to endpoint without further processing.

Peripheral NoC

The peripheral portion of the NoC carries transactions between the FPGA core and the peripheral IP blocks. The NoC can also carry transactions directly between the different peripheral IP blocks. The NoC provides the following services:

- Address decoding
- Transaction command and response routing
- Width adaptation
- Frequency adaptation (clock domain crossing)
- Burst adaptation
- Protocol conversion (e.g., AXI to/from APB)

The peripheral portion of the NoC only carries read and write transactions. It does not carry Ethernet packets or data from SerDes.

Each row of the NoC presents an AXI master to the periphery of the NoC on both the west and east side of the FPGA core. Similarly, each column of the NoC presents an AXI slave to the periphery of the NoC on both the north and south side of the device. This structure allows user logic to read or write any external IP or control and status register (CSR) interface and allows any external IP with a master interface to access any slave endpoints with attached user logic.

The NoC on a Speedster7t FPGA has two important features:

- The NoC is usable immediately when reset is released, without configuration of any control and status registers, the FPGA fabric, or the IP interfaces.
- After configuration of IP interfaces and/or control and status registers, the NoC supports transfers between IP cores (such as PCIe and GDDR6) without requiring the FPGA fabric to be configured.

Connectivity Between NoC and Endpoints on FPGA

The connectivity between the NoC and the different endpoints on the FPGA device can be categorized into three scenarios: NoC-to-user logic connectivity, NoC-to-interface IP connectivity, and NoC-to-FCU connectivity.

NoC-to-User Logic Connectivity

A NoC access point (NAP) needs to be instantiated in the user design in order to gain access to the rows and columns of the NoC. There is a NoC column with a master NAP and a slave NAP in each cluster. To the FPGA core, these access points look like any other logic columns in the FPGA fabric. The FPGA core provides a clock to the NAP as it does for any other column type. Internally, the NAP has an asynchronous FIFO used to adapt the data rates to what the FPGA can achieve.

NoC-to-Interface IP Connectivity

The NoC enables any NoC access point (NAP) in the FPGA to access any Interface IP slave, including any of the GDDR6 AXI interfaces and any of the DDR4/5 or PCIe controllers. It is also feasible to access the control and status interfaces of every IP core, DLL/PLL, and the FCU, through the NoC.

DDR4/5 and GDDR6 Connectivity

Each memory interface presents a 256-bit slave interface to the NoC and accepts read or write transactions. Multiple NoC access points can issue transactions to a single memory interface to utilize the full bandwidth provided by the high-speed memory interfaces.

PCI Express Connectivity

PCIe masters and slaves are connected directly to the NoC.

PCIe TLP interfaces are not connected to the NoC, but instead connected directly to the FPGA input and output pins.

NoC-to-FCU Connectivity

The fabric configuration unit (FCU) can issue transactions to the NoC, allowing the configuration logic to set any CSR interface on the device. Agents on the NoC, such as FPGA logic and the PCIe master can issue commands to the FCU, allowing for configuration over PCIe and other useful features.

Chapter - 5: Speedster7t FPGA IP Interfaces

The Speedster7t FPGAs have dedicated, hard interfaces to support the latest and most advanced versions of serial and memory interfaces used in high-performance networking and compute offload applications including 400G Ethernet, PCI Express Gen5, GDDR6, and DDR4 or DDR5. The combined interfaces exceed 10 terabits per second of total device bandwidth.

Ethernet

Speedster7t FPGAs include an Ethernet subsystem consisting of 8 SerDes lanes and Ethernet MACs to support a combination of applications. The Ethernet MAC is very flexible and can support multiple ports up to 400G, with each SerDes lane able to achieve a line rate between 10G and 100G. The Ethernet subsystem connects to the FPGA fabric through the network on chip (NoC). The table below lists the supported applications.

Table 9: ***Ethernet Supported Modes***

Mode	SerDes Lanes	SerDes Rate (Per Lane)	Description
400G	8	50G	400G over 8 lanes
	4	100G	400G over 4 lanes
200G	4	50G	200G over 4 lanes
	2	100G	200G over 2 lanes
100G	4	25G or 26.5G	100G over 4 lanes (RSFEC-KR4 or RSFEC-KP4)
	2	50G	100G over 2 lanes
	1	100G	100G over 1 lane
10/25/40/50G	2	25G	50G over 2 lanes
	1	50G	50G over 1 lane
	4	10G	40G over 4 lanes

Table 10: ***Multi-rate Supported Modes***

Mode	Number of Channels	SerDes Rate (Per Lane)	Description
10G/25G/50G/100G	Up to 8	10G, 25G, 50G, 100G	Independent single-lane applications
50G	Up to 4	25G	2 lanes each channel

Mode	Number of Channels	SerDes Rate (Per Lane)	Description
100G	Up to 2	25G	4 lanes each channel
	Up to 4	50G	2 lanes each channel
200G	Up to 2	50G	4 lanes each channel
	Up to 4	100G	2 lanes each channel
400G	Up to 2	100G	4 lanes each channel
	1	50G	8 lanes

Additional Features

- Support for RS(528, 514) (KR) codewords and RS(544, 514) (KP) depending on mode of operation
- Support for RS(272, 256) for at least up to 100G
- Support for 15G (Clause 108) and 50G (Clause 134) and 25/50G Ethernet Consortium specifications
- Support for error indication to PCS when uncorrectable errors are detected
- 1588 I-step for 10G up to 100G
- The IEEE 802.3br supported, providing two transmit and receive interfaces for 10G up to 100G
- 1588 I-step for 200G and 400G
- TSN support for 100G and below (IEEE 802.1 Time Sensitive Networking, and IEEE 802.3br Interspersing Express Traffic)
- Interface for register configuration

PCI Express

Speedster 7t FPGAs have two PCIe interfaces. The first interface supports up to 16 lanes (×16). The second PCIe interface supports up to 8 lanes (×8). Both PCIe controller interfaces support dual-operation, as either an endpoint or as a root complex.

Table 11: *Speedster7t PCIe Interface Specifications*

Feature	PCIe Port 1	PCIe Port 2
PCI Express Specification	Revision 5.0, Version 0.9	Revision 5.0, Version 0.9
PIPE	Version 5.1.1	Version 5.1.1
Maximum width	×16	×8
Maximum throughput	512 GTs (Gen 5)	256 GTs (Gen 5)
Supported functionality	Root-Port + End-Point	Root-Port + End-Point

Feature	PCIe Port 1	PCIe Port 2
DMA support	Yes	Yes
DMA read channels	4	2
DMA write channels	4	2
BAR	4	4
Virtual channels	1	1
Physical functions	4	2
Virtual functions	252	0
Advanced error reporting (AER) support	Yes	Yes
IOV	256	None

GDDR6

Speedster7t devices contain GDDR6 interfaces on the west and east sides of the device to provide external high-bandwidth memory interface support. The controller and PHY implementation are compliant with the JEDEC GDDR6 SGRAM Standard JESD250. See the table below for a summary of the key specs and features.

Each GDDR6 interface operates on two channels, each of which can be disabled independently. The controller supports a wide range of features, including bus utilization optimization, page-hit mitigation, multiport front end (MPFE), reordering and error interrupt.

The GDDR6 interfaces can be run up to a data rate of 16 Gbps with device densities from 8 Gb to 16 Gb. The implementation supports GDDR6 up to ×16 in clamshell modes and up to ×8 in non-clamshell modes.

The GDDR6 controller connects to the other IP interfaces on the Speedster7t device or directly to the FPGA fabric via an AXI interface with support for full or half-rate clocking. The two options fabric or IP interface connectivity are through:

- A 256-bit AXI interface to the network on chip (NoC), which can run up to 1 GHz.
- A 512-bit AXI direct-to-fabric interface, which can run up to 500 MHz.

Users can configure the PHY ZQ calibration as Master/Slave mode across multiple PHY’s.

Furthermore, the IP comes with a memory test and analyzer core to enable standalone testing of the controller and memory during board bring up.

Table 12: ***GDDR6 Key Specs and Features on Speedster7t***

GDDR6 Feature	Support in Speedster7t Devices
Memory suppliers	Micron, Samsung, SK Hynix
Maximum number of memory chips per FPGA	8 (non-clamshell), 16 (clamshell)
Maximum total capacity	16GB (1×16 Gb chips in non-clamshell mode) 16GB (2×8 Gb chips in clamshell mode)
Number of channels per chip	2
Maximum number of channels total per FPGA	16
Width per channel (bits)	16
Maximum per-pin data rate supported by FPGA	16 Gbps
Maximum total bandwidth (No_of_channels_per_FPGA × width_per_channel × rate)	4.0 Tbps
Capacity per memory chip	4 Gb, 8 Gb, 12 Gb, 16 Gb
Total memory per FPGA	Up to 16GB
Memory data rates	12 Gbps, 14 Gbps, 16 Gbps

DDR4/DDR5

Speedster7t devices include DDR5 interfaces (DDR4 in the AC7t1500), ensuring that memory capacity requirements can be satisfied across a vast application space. The DDR4/5 PHY and controller in Speedster7t devices are compliant to the DDR4/5 JEDEC specification and can operate up to 3200 Mbps in ×4, ×8 and ×16 width configurations. The implementation supports component memories, UDIMM/SO-DIMM form factors as well as RDIMMs and LRDIMMs. See the table below for a summary of the key specifications and features.

Speester7t devices allow for multi-rank support in the DDR4/5 interfaces, up to 4 in standard mode, and up to 16 in 3DS mode.

The DDR4/5 PHY/controller connects to the SoC or FPGA fabric via an AXI interface with support for full, half and quarter-rate clocking. The two options fabric/SOC connectivity are through:

- A 256-bit AXI interface to the external network on chip (eNoC), which can run up to 800 MHz.
- A 512-bit AXI direct-to-fabric interface, which can run up to 400 MHz.

Speedster7t devices support AXI compliant low-power interfacing. The DDR4/5 PHY/controller provides three options for low-power mode:

- 256-bit AXI interface in low power
- 512-bit AXI interface in low power

- Memory controller core logic in low power

Users also have the option to bypass the entire DDR4/5 PHY and use these I/O for driving low-performance interfaces such as I^2C, or for optics control, LEDs, etc.

Table 13: ***DDR4/5 Key Specifications and Features on Speedster7t Devices***

DDR4/5 Feature		Support in Speedster7t Devices
Memory types		Component, UDIMM/SO-DIMM, RDIMM, LRDIMM
Memory configurations		×4, ×8, ×16
Maximum data rate		3200 Mbps
Burst modes		BL8, burst chop
Data path widths	Non-ECC	8-bit, 16-bit, 32-bit, 64-bit
	ECC	32-bit + 7-bit ECC, 64-bit + 8-bit ECC
Multi-rank support		4 (standard), 16 (3DS)
AXI interface		AXI4 with read reorder buffer and port data widths of 256 and 512 bits
Testability and characterization		Built-in scan, loopback, delay line, PLL, auto-timing and ATE read tests.

Chapter - 6: Speedster7t FPGA Configuration

For normal operation, the Speedster7t FPGA core requires configuration by the end user. Speedster7t devices can be configured via one of four interfaces:

- PCI Express
- CPU
- JTAG
- Flash

A configuration bitstream is generated by ACE by selecting the appropriate configuration interface (bitstreams are configuration interface specific). The configuration mode of the FPGA is controlled via the configuration interface of the FPGA. These pins can be driven via hardware on the board or by another device such as a CPLD. The user has the option to generate an encrypted and authenticated bitstream. If this feature is used, the Speedster7t device first secures the hardware and then authenticates and decrypts the bitstream before programming the FPGA fabric.

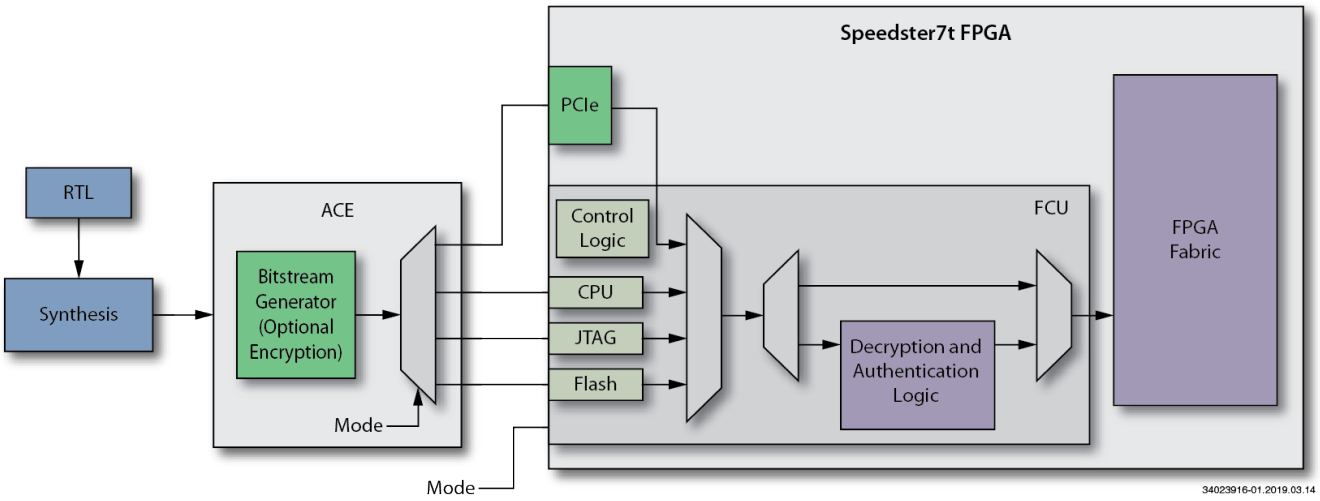

Figure 9: *Bitstream Generation and Configuration Process*

CPU Mode

In CPU mode, an external CPU acts as the master and controls programming operations. This mode offers a high-speed method for loading configuration data. Depending on the pin settings, CPU mode is either a 1-, 8-, 16-, 32-, or 128-bit wide parallel interface. This mode provides for the widest data interface and a maximum supported clock rate of 250MHz.

PCIe Mode

PCIe programming is performed via indirect addressing, where the AXI slave interface in the Speedseter7t FPGA receives the bitstream in the form of a PCIe packet and writes that data to the programming registers.

JTAG Mode

The Speedster7t JTAG Tap controller is IEEE Std 1149.1 and 1149.6 (AC JTAG) compliant. The JTAG interface also provides debug capability for Snapshot and other debug tools. The Speedster7t FPGA can be configured as a single JTAG device, or as part of a series of cores within a system connected on the JTAG chain.

Flash Mode

The serial flash programming mode allows flash memories to be used to configure the Speedster7t FPGA. In this mode the Speedster FPGA is the master, and therefore, supplies the clock to the flash memory. Flash programming supports SPI (single-bit interface to the flash memory), dual (two-bit interface to the flash memory), quad (four-bit interface to the flash memory) and octa (eight-bit interface to the flash memory) modes. Additionally, the Speedster7t FPGA can interface to one (×1) or four (×4) flash memory modules on the board. The bitstream size is entirely dependent on the size of the fabric. It is important that the flash solution chosen is large enough to store the bitstream data.

Flash mode also supports the remote update feature, wherein the user can simultaneously store two bitstreams in the flash device and choose to program the FPGA from either one. The update can be triggered remotely via a user application that writes to appropriate registers on the Speedster7t device.

Bitstream Security Features

Achronix recognizes the importance of protecting sensitive IP a customer downloads onto their FPGA. To that extent, Speedster7t FPGAs have a number of features to support bitstream encryption as well as authentication. These features ensure that no one can see the design on the FPGA and also ensures that the design is the correct design. Speedster7t FPGAs provide this high level of security through the following features:

- Support for AES encrypted and authenticated bitstream
- DPA protection to prevent side-channel attacks
- Physically unclonable function (PUF) for tamper-proof protection
- Securely stores both public and encrypted private keys

With this security solution deployed, a customer's design is secure. Even with possession of the device, no one can extract the underlying design, the design cannot be reverse engineered, nor can the design be altered in any way.

Chapter - 7: Speedster7t FPGA Debug

JTAG Browser View

The JTAG Browser view provides the user with an interactive means of inspecting and modifying registers within the active design on an FPGA over the JTAG interface. (The acx_stapl_player and Bitporter pod or FTDI FT2232H JTAG device perform the JTAG interactions; see the *Bitstream Programming and Debug User Guide (UG004)* for more information.)

After choosing the Target Device and the IP Block within that device, the user is able to browse and edit registers on a live device. All accessible IP blocks on the FPGA are selectable from a pull down list; once selected, the attributes (base-address, end-address, word-size, etc) for the selected IP block are displayed, along with the acx_stapl_player commands which will be used to read and write to the block's registers.

Snapshot

Snapshot is the real-time design debugging tool for Achronix FPGAs and cores. The Snapshot debugger, which is embedded in the ACE software, delivers a practical platform to observe the signals of a user's design in real-time. To use the Snapshot debugger, the Snapshot macro needs to be instantiated inside the user's RTL. After instantiating the macro and programming the device, the user will be able to debug the design through the Snapshot Debugger GUI within ACE, or via the `run_snapshot` TCL command API.

The Snapshot macro can be connected to any logic signal mapped to the Achronix core, to monitor and potentially trigger on that signal. Monitored signal data is collected in real time in regular BRAMs, prior to being transferred to the ACE Snapshot GUI. The Snapshot macro has configurable monitor width and depth, as well as other configuration parameters, to allow user control over resource usage. The ACE Snapshot GUI interacts with the hardware via the JTAG interface: interactively specified trigger conditions are transferred to the design, and collected monitor data is transferred back to the GUI, which displays the data using a builtin waveform viewer.

The figure below shows the components involved in a Snapshot debug session.

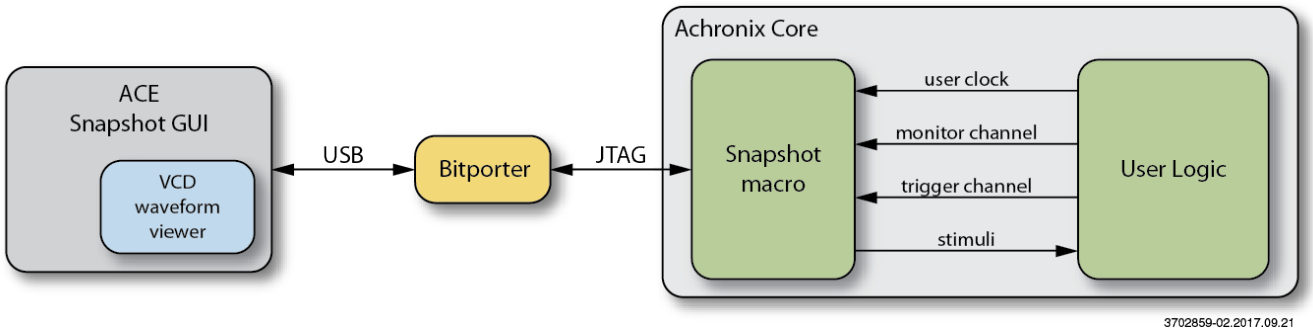

Figure 10: *Snapshot Overview*

Features

The Snapshot macro samples user signals in real time, storing the captured data in one or more BRAMs. The captured data is then communicated through the JTAG interface to the ACE Snapshot GUI.

The implementation supports the following features:

- Monitor channel capture width of 1 to 4064 bits of data.
- Monitor channel capture depth of 512 to 16384 samples of data at the user clock frequency.
- Trigger channel width of 1 to 40 bits.
- Supports up to three separate sequential trigger conditions. Each trigger condition allows for the selection of a subset of the trigger channel, with AND or OR functionality.
- Bit-wise support for edge- (rise/fall) or level-sensitive triggers.
- The ACE Snapshot GUI allows specification of trigger conditions and circuit stimuli at runtime.
- An optional initial trigger condition, specified in RTL parameters, to allow capture of data immediately after startup, before interaction with the ACE Snapshot GUI.
- A stimuli interface, 0 to 512 bits wide, that allows the user to drive values into the Achronix core logic from Snapshot. Stimuli values are specified with the ACE Snapshot GUI and made available before data capture.
- Optionally, the data capture can include values before the trigger occurred. This "pre-store" amount can be specified in increments of 25% of the depth.
- Captured data is saved in a standard VCD waveform file. The ACE Snapshot GUI includes a waveform viewer for immediate feedback.
- The VCD waveform file includes a timestamp for when the Snapshot was taken.
- ACE automatically extracts the names of the monitored signals from the netlist, for easy interpretation of the waveform.
- A repetitive trigger mode, in which repeated Snapshots are taken and collected in the same VCD file.
- The JTAG interface can be shared with the user design.
- A TCL batch/script mode interface is provided via the `run_snapshot` TCL command

Chapter - 8: Speedster7t FPGA Speed Grades and Power Rails

Table 14: *Speedster7t Speed Grade and Temperature Grade*

Speed Grade	-40°C to +105°C	
	Nominal Voltage (V)	Relative Performance
C1	0.90	1.56x
C2	0.85	1.25x
C3L	0.75	1.00x

Achronix's Speedster7t devices have an operating lifetime of ten years and can support the following temperature grades:

- Commercial (0°C to +85°C)
- Industrial (-40°C to +100°C)

The temperature support beyond 100°C allows applications that require support up to 105°C to be accommodated.

Table 15: *Speedster7t Power Supply Requirements*

Symbol	Description	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple
GDDR_VDDR	Power supply 1 for the GDDR6 PHY	0.765	0.85	0.935	
GDDR_VDDIO	Power supply 2 for the GDDR6 PHY	1.22	1.35	1.42	
DDR_VDDQ	Output stage drain power supply for the DDR4/5 PHY	1.14	1.2	1.26	±2.5%
PLL_FUSE_VDDA	Analog supply for the DDR4/5 PHY	1.71	1.8	1.89	±2.5%
	Analog supply for the general purpose PLLs				
	Analog supply for the eFUSE module				

Table 16: *Speedster7t Power Supply Requirements (cont.)*

Symbol	Description	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple
PA_VDDH	High analog supply for the SerDes PMA	1.08	1.2	1.32	30 mVpk-pk ≥ 1 KHz 15 mVpk-pk ≥ 10 MHz
PA_VDDL	Low analog supply for the SerDes PMA	0.675	0.75	0.825	30 mVpk-pk ≥ 1 KHz 15 mVpk-pk ≥ 10 MHz
FCU_CB_VDDIO	Analog supply for the GPIO associated with FCU/JTAG	1.62	1.8	1.98	
VDDIO	Analog supply for the MSIO IO /DIFF I/O (1.1V nominal)	0.99	1.1	1.21	
	Analog supply for the MSIO IO /DIFF I/O (1.2V nominal)	1.08	1.2	1.32	
	Analog supply for the MSIO IO /DIFF I/O (1.35V nominal)	1.215	1.35	1.485	
	Analog supply for the MSIO IO /DIFF I/O (1.5V nominal)	1.35	1.5	1.65	
	Analog supply for the MSIO IO /DIFF I/O (1.8V nominal)	1.62	1.8	1.98	
VDDL	Power supply for the FPGA fabric (C3L)	0.675	0.75	0.825	
	Power supply for the FPGA fabric (C2)	0.765	0.85	0.935	
	Power supply for the FPGA fabric (C1)	0.81	0.9	0.95	
VCC	Digital supply for the GDDR6 controller	0.6750	0.750	0.825	
	Digital supply for the DDR4/5 controller				
	Digital supply for the DDR4/5 PHY				

Table 17: *Speedster7t Power Supply Requirements (cont.)*

Symbol	Description	Minimum Voltage (V)	Typical Voltage (V)	Maximum Voltage (V)	AC Ripple
VCC	Digital supply for the Achronix PCS	0.675	0.750	0.825	
	Digital supply for the eFUSE module				
	Digital supply for the GPIO FCU /JTAG logic				
	Digital supply for the SOC Ethernet controller				
	Digital supply for the SOC PCIe controller				
	Digital supply for the SOC NoC				
	Digital supply for the PLLs/DLLs				
	Digital supply for the MSIO core				
	Digital supply for the DIFF IO core				
	Digital supply for the SerDes				

Revision History

The following table lists the revision history of this document.

Version	Date	Description
0.9	28 Mar 2019	• Preliminary alpha release.
0.91	05 Jun 2019	• Feature Summary (see page 7): Updated DDR4/5 features. • Family Features (see page 8): Updated Table: Speedster7t Family Overview (see page 8). • Family Features (see page 8): Updated Table: Speedster7t Package and I/O Combinations (see page 8). • Family Features (see page 8): Updated Figure: Speedster7t1500 Top-Level Block Diagram (see page 10). • Machine Learning Processing (MLP) Block (see page 13): Updated feature details. • Speedster7t FPGA I/O and PHY (see page 22): Updated minor details in PLLs (see page 24). • Speedster7t FPGA Network On Chip (see page 26): Updated minor feature details. • Speedster7t FPGA IP Interfaces (see page 31): Updated DDR4/DDR5 (see page 34). • Speedster7t FPGA Speed Grades and Power Rails (see page 40): Updated Table: Speedster7t Speed Grade and Temperature Grade (see page 40).
0.92	24 Jun 2019	• Removed confidential marking.